AMENDMENTS TO THE CLAIMS

The present listing of claims replaces all prior versions and listings of claims in the subject patent application.

Listing of Claims:

Claim 1 (previously presented): An integrated circuit having a plurality of circuits formed on a common substrate that are isolated by isolation regions in said common substrate between said circuits, said integrated circuit made by the process of:

masking predetermined locations of said common substrate that are aligned with said isolation regions with a material that is capable of masking high energy ions;

irradiating said common substrate with said high energy ions such that said high energy ions have an energy level sufficient to implant said high energy ions in embedded regions of said common substrate that have a lower resistance than said common substrate and that are substantially aligned with unmasked portions of said common substrate that are substantially aligned with said circuits so that said isolation regions having a higher resistance than said common substrate are formed in said common substrate between said embedded regions and said embedded regions are buried in said common substrate so that currents injected into said common substrate by said circuits preferentially flow to a ground potential rather than through said isolation region.

Claim 2 (currently amended): An integrated circuit comprising:

a common substrate having low doping and a first predetermined resistance;

circuitry formed on predetermined portions of said common substrate;

embedded regions of said common substrate that are implanted with ions such that said embedded regions have a resistance that is lower

than said first predetermined resistance, said embedded regions being substantially aligned with said circuitry and buried in said common substrate so that currents injected into said common substrate by said circuits preferentially flow to a ground potential ~~rather than through said isolation region~~.

Claim 3 (original): The integrated circuit of claim 2 wherein said common substrate includes an epitaxial layer and a substrate layer.

Claim 4 (original): The integrated circuit of claim 2 wherein said embedded regions form a checkerboard pattern.

Claim 5 (original): The integrated circuit of claim 2 wherein said implanted ions comprise boron ions.

Claim 6 (original): The integrated circuit of claim 2 wherein said implanted ions comprise phosphorous ions.

Claim 7 (currently amended): A silicon wafer suitable for the formation of integrated circuits comprising:

a common substrate on which said integrated circuits can be formed in predetermined locations on said common substrate, said common substrate having a first predetermined resistance;

embedded regions of implanted ions deposited in said common substrate that are substantially aligned with said predetermined locations on said common substrate, said embedded regions having a resistance that is lower than said first predetermined resistance and buried in said common substrate so that currents injected into said common substrate by said circuits preferentially flow to a ground potential ~~rather than through said isolation region~~.

Claim 8 (original): The silicon wafer of claim 7 wherein said common substrate includes an epitaxial layer and an underlying substrate layer.

Claim 9 (previously presented): An integrated circuit formed on a common substrate of a wafer made by the process of:

masking locations on a said wafer;

irradiating said wafer with ions having an energy level sufficient to implant said ions in embedded regions of said common substrate so that a portion of said embedded regions are substantially aligned with unmasked portions of said wafer and said embedded regions are buried in said common substrate that have a lower resistance than said common substrate and isolation regions having a higher resistance than said common substrate are formed between said embedded regions so that currents injected into said common substrate by said circuits preferentially flow to a ground potential rather than through said isolation region.

Claim 10 (previously presented): An integrated circuit formed on a common substrate of a wafer made by the process of:

forming a mask in locations on said wafer;

irradiating said wafer with ions in the range of approximately 1 MeV to 3 MeV to implant said ions in embedded regions of said common substrate that have a lower resistance than said common substrate so that isolation regions that have a higher resistance than said common substrate are formed between said embedded regions so that currents injected into said common substrate by circuits substantially aligned with said embedded regions preferentially flow to a ground potential rather than through said isolation regions.

Claim 11 (previously presented): An integrated circuit having a common substrate and isolation regions between circuits formed on said integrated circuit made by the process of:

masking regions of said common substrate, that correspond to said isolation regions, with a masking material that is capable of masking high energy ions;

irradiating said integrated circuit with said high energy ions to produce implanted regions of said ions in said common substrate that have low resistivity compared to said isolation regions in said common substrate that are masked to prevent deposition of ions so that current injected into said common substrate by said circuits preferentially flows to a ground potential rather than through said isolation regions;

forming said circuits on said integrated circuit so that said circuits are substantially aligned with said implanted regions and said isolated regions are located between said circuits that are not substantially aligned with said circuits.